REMARKS

Claims 1 and 4-13 were presented for examination. Of these, claims 11-13 were allowed and the remaining claims were rejected. Applicant has confirmed by telephone with the Examiner that paragraph 1 on page 4 of the Office Action erroneously indicates that claims 5 and 8-9 were allowed. In response, and to further the prosecution of the application, Applicant hereby cancels claim 6 without prejudice, and requests reconsideration of the remaining rejections.

Claims 1, 4-5, 7-9 and 10 were rejected as anticipated by Itoh. The Examiner has acknowledged Applicant's arguments filed in October, 2005 but has indicated that they were not persuasive. The Examiner has suggested that Itoh does disclose in Figures 1 and 2 the claimed symmetrical layout structure of the claimed FET. The Examiner, however, is incorrect. Therefore, the rejection should be withdrawn.

The Office Action asserts that Fig. 1 of Itoh shows the control gate 39 between the source/drain 36 and the drain/source 40 and concludes that this meets the symmetry limitation. The Office Action further asserts that "the layer structure in Fig. 1 (the bird view picture) clearly shows the symmetrical FET 39." That is not true. Itoh was not particularly consistent in his language or use of reference numbers, and his drawings lack important details.. In Fig. 2, element 34 supposedly indicates a MOSFET (Col. 1, lines 28-29). But it appears that in Fig. 1, 34 points to the channel of the MOSFET. In Fig. 2, element 39 identifies a terminal connected to the gate of that MOSFET but in Fig. 1, 39 identifies a metallization layer which forms the gate itself. The text (Col. 1, lines 36-37) refers to 39 as a write word line. In Fig. 1, the channel 34 is formed under the gate 39 and to the right of channel 34 is a drain or source region labeled DS1 by Applicant. A contact metallization 40 connects to the region DS1 and provides a first data line. To the left of channel 34 in Fig. 1 is a charge storage layer 35 (Col. 1, line 38) which (as shown in Fig. 2) acts as the gate for a second MOSFET (indicated by numeral 33 in Fig. 2). In Fig. 1, numeral 33 identifies the bottom of the channel of such MOSFET. In Fig. 1, the cross-sectional view on the bottom does not make it at all clear where the drain and source regions are

but it would appear from the top view that they are disposed orthogonally with respect to the drain and source of the first transistor.

With respect to the second transistor (labeled 33 in Fig. 2), it is not even clear where the transistor is formed. Charge storage layer 35 rests on a thin oxide layer 32 over a portion of substrate 31, indicated by numeral 33. No source or drain electrodes are shown anywhere. Element 37 is supposed to refer to a read bit line and per Fig. 2 should connect to either the drain or source of MOSFET 33, and the other of the drain or source should be connected to a terminal receiving the second select signal, 38. However, it appears at the top of Fig. 1 that elements 37 and 38 are directly connected together! If that is not the case, the drawing is at very least quite ambiguous.

No information is provided as to either (1) the geometries or (2) the dopings of the source and drain regions of either of the transistors. Yet the claimed electrical symmetry, allowing the source and drain to be interchanged and signal to flow in either direction interchangeably, would require both substantially symmetrical physical geometry and substantially symmetrical doping. If one looks at the sectional view at the bottom of Fig. 1, it is apparent with respect to the first transistor, labeled 34 in Fig. 2, that, in fact, the drain and source geometries are very different.

Manifestly, one cannot determine from Fig. 1 that either transistor employs a geometrically or electrically symmetrical structure. The Examiner is entirely speculating in that respect. However, speculation may not be the basis for an anticipation rejection. The reference must clearly teach the claimed invention. It does not. Accordingly, the rejection should be withdrawn.

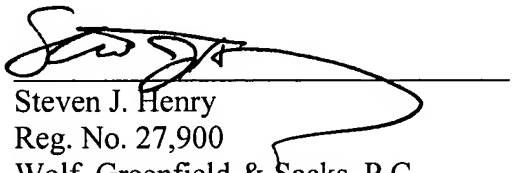
There simply is no disclosure in Itoh et al of the claimed invention. The Examiner improperly reads into Itoh et al limitations taught only by Applicant.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,



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